ABSTRACT

A self-testing and correcting read only memory (RAM) device and methodology is disclosed herein. The device includes at least one array of memory to enable data storage and self-testing RAM interface for evaluating, correcting, and/or compensating for memory cell errors. The RAM device, *via* the self-testing RAM interface, supports interaction with a central processing unit (CPU) to facilitate testing of the CPU to memory interface as well as the device memory array. Upon detection of memory errors, the self-testing RAM interface can notify the CPU, notify an exception handler, correct, and/or compensate for the errors. Error correction can be accomplished using error correction codes (ECCs) alone or in combination with retrieval and replacement of erroneous data with correct data stored in different locations. Memory cells that are physically defective and incapable of maintaining data integrity can be compensated for by mapping defective cells to a plurality of reserved replacement cells.